REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 11, 12, and 31-36 are pending in the present application. Claim 11 is amended, Claims 1-10 and 13-30 are canceled without prejudice, and Claims 31-36 are added by the present amendment.

In the outstanding Office Action, Claim 11 was rejected under 35 U.S.C. § 103(a) as unpatentable over Verrett (U.S. Patent No. 5,612,243) in view of Korean Patent Application Laid-Open No. 1996-0002744 (herein "'744") and Applicants' admitted art (AAA), and Claim 12 was rejected under 35 U.S.C. § 103(a) as unpatentable over Verrett in view of '744 and AAA.

Applicants thank the Examiner for the courtesy of an interview extended to Applicants' representative on November 18, 2004. During the interview differences between the claims and the applied art were discussed. Further, clarifying claim amendments and new claims, similar to those presented herewith, were also discussed. No agreement was reached, pending the Examiner's detailed consideration of the claims and upon formal submission. Arguments presented during the interview are reiterated below.

The specification has been amended to correct minor informalities and the Abstract has been replaced with a new Abstract that is consistent with amended Claim 11. No new matter has been added.

Regarding the rejection of Claim 11 under 35 U.S.C. § 103(a) as unpatentable over Verrett in view of '744 and AAA, Claim 11 has been amended to recite a surface of a semiconductor layer is silicidized in such a state that a surface of an isolation film is exposed. The claim amendment finds support in Figures 32 and 35. No new matter is believed to be

added. Because the AAA has not been used against Claim 11 although AAA was listed in the body of the present rejection, Applicants believe that AAA was listed in error in the present rejection.

Briefly recapitulating, Claim 11 is directed to a semiconductor device that includes a semiconductor layer, a plurality of semiconductor elements formed on the semiconductor layer, an isolation film provided in a surface of the semiconductor layer, and a PN junction portion formed by two semiconductor regions of different conductivity types in the semiconductor layer. The isolation film electrically isolates the semiconductor elements from each other and includes a nitride film, and upper oxide film, and a lower oxide film, and the upper oxide film and the lower oxide film are provided in upper and lower portions of the nitride film. The surface of the semiconductor layer is silicidized in such a state that a surface of the isolation film is exposed

In a non-limiting example, Figure 32 shows the semiconductor device 303 having the semiconductor layer 10, the semiconductor elements LR and PR, the isolation film ST35, and the PN junction JP.

Turning to the applied art, '744 discloses a structure that increases the size of a cell region by minimizing an element isolation region. The structure has a laminated element isolation film of oxide film-nitride film-oxide film formed within a trench provided on a silicon substrate. However, '744 does not teach or suggest providing the element isolation film in a position corresponding to a top of a PN junction and silicidizing the semiconductor substrate in such a state that a surface of the isolation film is exposed, as required in amended Claim 11.

Further, the element isolation film of '744 adopts a laminated structure of oxide film-nitride film-oxide film because of the isolation characteristic of this combination of films and

not to prevent, with the nitride film, a diffusion of a metal formed on the isolation film during a silicide process.

Thus, '744 is not concerned with the silicide process, and does not recognize the problem to prevent a metal silicide from being formed by metal diffusion in vicinity of a PN junction.

On the contrary, even if a metal layer of Claim 11 remains in a surface of the isolation film when a surface of the semiconductor layer is silicidized and diffuses into the isolation film, the diffusion is prevented by the nitride film of the isolation film.

Verrett shows in Figure 4 a polysilicon layer 35 and a silicide layer 37 that remain on the isolation film 16b, and the surface of the isolation film 16b is not exposed as required by amended Claim 11. Moreover, because the polysilicon layer 35 of Verrett is formed on the isolation film 16b and the silicide layer 37 is further formed thereon, the metal pollution does not reach a PN junction, and therefore the problem of the metal pollution is not recognized by Verrett. Thus, neither '744 nor Verrett, either alone or in combination, teaches or suggests silicidizing a semiconductor substrate in such a state that a surface of an isolation film is exposed.

Accordingly, it is respectfully submitted that amended Claim 11 patentably distinguishes over Verrett and '744.

The rejection of Claim 12 under 35 U.S.C. § 103(a) as unpatentable over Verrett in view of '744 and AAA is respectfully traversed because neither '744 nor AAA overcomes the deficiencies of Verrett discussed above. In addition, Claim 12 depends from independent Claim 11, which is believed to be allowable as noted above. Accordingly, it is respectfully submitted that dependent Claim 12 is also allowable.

New independent Claims 31-36 have been added to set forth the invention in a varying scope and Applicants submit the new claims are readable on Species A and are supported by the originally filed specification. In particular, new independent Claim 31 recites the features of original Claim 11 and a "nitride film being completely buried within said semiconductor layer," new independent Claim 33 recites the features of original Claim 11 and "a metal layer formed over said semiconductor layer and said plurality of semiconductor elements such to expose said isolation film," new independent Claim 35 recites the features of original Claim 11 and "said isolation film having an upper surface flush with said surface of said semiconductor layer," and dependent Claims 32, 34, and 36 are identical to original Claim 12 but depend from Claims 31, 33, and 35, respectively. The added features find support for example in Figure 32. No new matter is believed to be added.

As discussed during the interview, the applied art does not teach or support the above discussed features. More specifically, regarding Claim 31, Verrett does not show a nitride film and '744 shows in Figure 4 that a nitride film is formed above the semiconductor layer 1 and not completely buried within the semiconductor layer 1. Regarding new Claims 33 and 35, Verrett shows in Figure 4 that a metal layer 37 completely covers the isolation film 16b instead of exposing the isolation film 16b as required in Claims 33 and 35. Accordingly, it is respectfully submitted new Claims 31-36 patentably distinguish over Verrett and '744, either alone or in combination.

Consequently, in light of the above discussion and in view of the present amendment, this application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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